CMOS 8-Bit Microcontroller

TMP87CC78F, TMP87CH78F, TMP87CK78F, TMP87CM78F

The 87CC78/H78/K78/M78 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain 8-bit A/D conversion inputs and a VFT (Vacuum Fluorescent Tube) driver on a chip.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CC78F	12 K × 8-bit	512 × 8-bit	P-QFP100-1420-0.65A	TMP87PM78F
TMP87CH78F	16 K × 8-bit			
TMP87CK78F	24 K × 8-bit	1024 × 8-bit		
TMP87CM78F	32 K × 8-bit			

Features

◆8-bit single chip microcomputer TLCS-870 Series
◆Instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
◆412 basic instructions
- Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits)
- Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
- 16-bit data operations
- 1-byte jump/subroutine-call (Short relative jump/ Vector call)

◆15 interrupt sources (External: 5, Internal: 10)
- All sources have independent latches each, and nested interrupt control is available.
- 3 edge-selectable external interrupts with noise reject
- High-speed task switching by register bank changeover

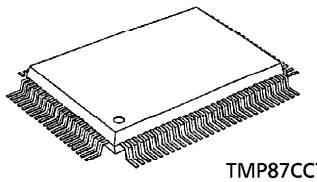
◆13 Input/Output ports (89 pins)
- Output: 2 port (16 pins)
- Input/Output: 11 ports (73 pins)

◆Two 16-bit Timer/Counters
- Timer, Event counter, programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes.

◆Two 8-bit Timer/Counters
- Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes

◆Time Base Timer (Interrupt frequency: 1 Hz to 16 kHz)
◆Divider output function (frequency: 1 kHz to 8 kHz)

P-QFP100-1420-0.65A



TMP87CC78F
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TMP87PM78F

◆Watchdog Timer
- Interrupt source/reset output (programmable)

◆8-bit Serial Interface: 2 channels
- With 8 bytes transmit/receive data buffer
- Internal/external serial clock, and 4/8-bit mode

◆8-bit successive approximate type A/D converter with sample and hold
- 8 analog inputs
- Conversion time: 23 μs at 8 MHz

◆Vacuum Fluorescent Tube Driver (automatic display)
- High breakdown voltage ports (max. 40 V × 50 bits)

◆Key scanning function
- Key-matrix constructed by segment outputs (1 to 16) and key inputs (1 to 8)

◆Dual clock operation
- Single/Dual-clock mode (option)

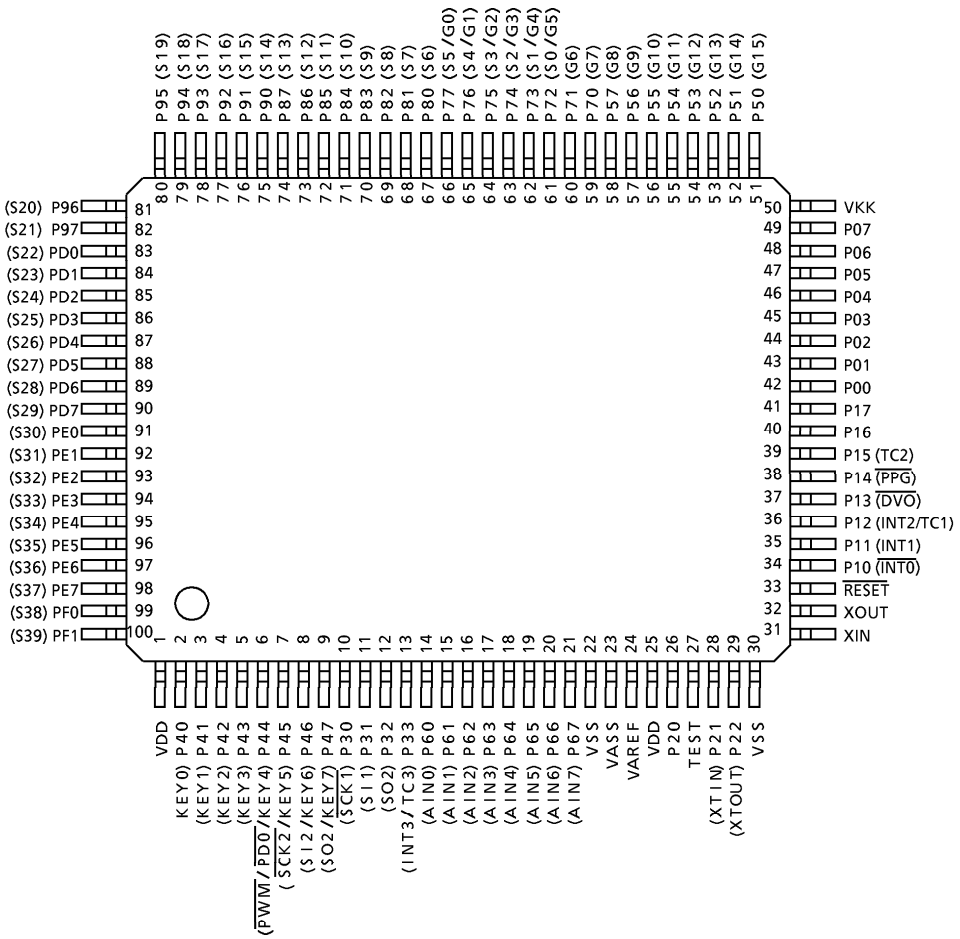
◆Five Power saving operating modes
- STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
- SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz).
- IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- IDLE2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupts.
- SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.

◆Wide operating voltage: 2.7 to 5.5 V at 32.768 kHz, 4.5 to 5.5 V at 8 MHz / 32.768 kHz

◆Emulation Pod: BM87CM78F0A

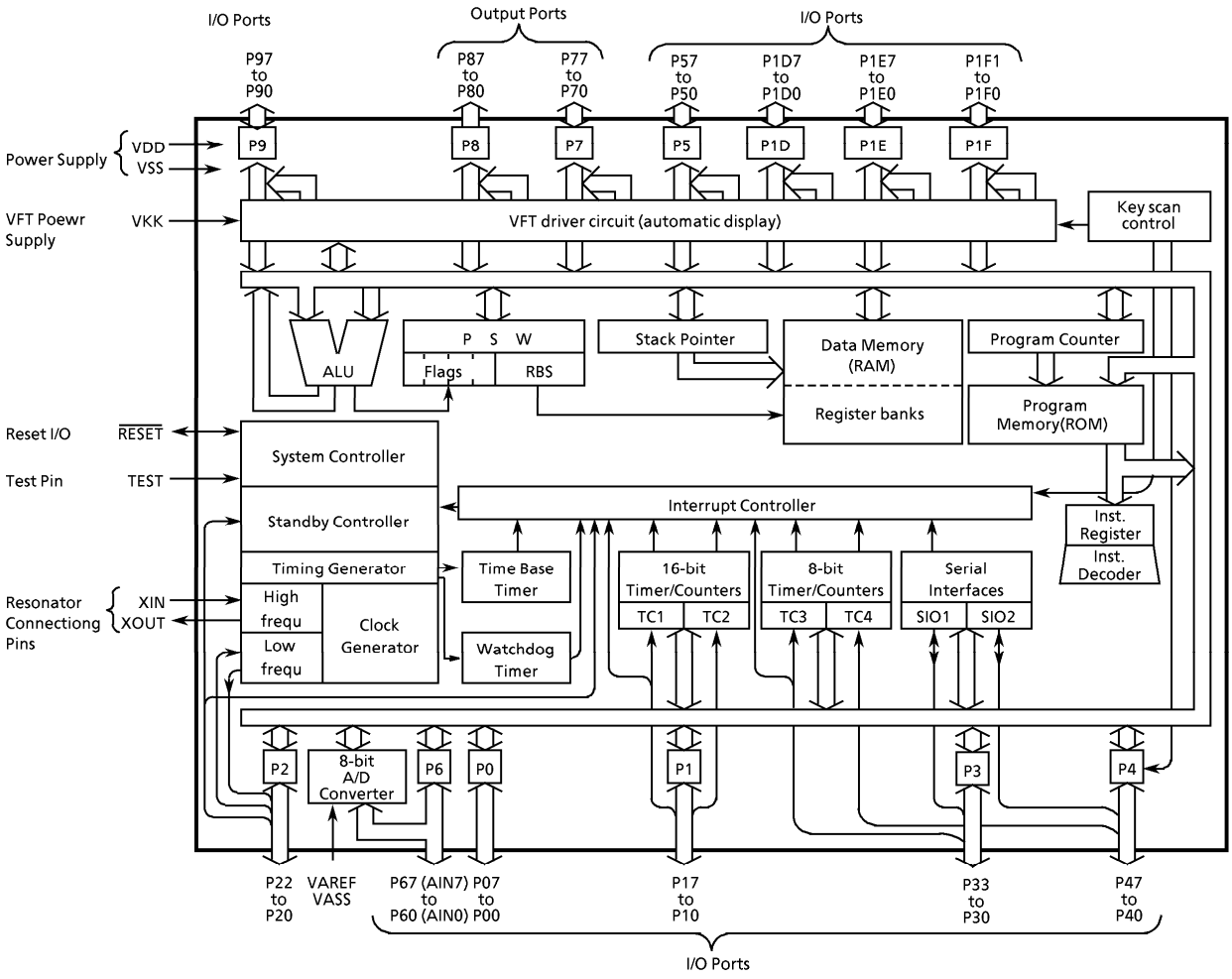
Pin Assignments (Top View)

P-QFP100-1420-0.65A



Note: All VDDs should be connected externally for keeping the same voltage level.

Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P07 to P00	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as inputs. When used as a divider output, the latch must be set to "1".	
P17, P16	I/O		
P15 (TC2)	I/O (Input)		Timer/Counter 2 input
P14 ($\overline{PPG}$)	I/O (Input)		Programmable pulse generator output
P13 ($\overline{DVO}$)	I/O (Input)		Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{INT0}$)			External interrupt input 0
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, the latch must be set to "1".	Resonator connecting pins (32.768 kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$/$\overline{STOP}$)			External interrupt input 5 or STOP mode release signal input
P33 (INT3 / TC3)	I/O (Input)	4-bit input/output port with latch. When used as an input port, a SIO input/output, a timer/counter input, or an interrupt input, the latch must be set to "1".	External interrupt input 3 or Timer/Counter 3 input
P32 (SO1)	I/O (Output)		SIO serial data Output1
P31 (SI1)	I/O (Input)		SIO serial data Input1
P30 ($\overline{SCK1}$)	I/O (I/O)		SIO serial clock input/output
P47 (SO2/KEY7)	I/O (I/O)	8-bit input/output port with latch. When used as an input port, a SIO Input/Output, or a PWM/PDO output, the latch must be set to "1".	SIO Serial data output2 or key scan input7
P46 (SI2 / KEY6)	I/O (Input)		SIO Serial data input2 or key scan input6
P45 ($\overline{SCK2}$ / KEY5)	I/O (I/O)		SIO Serial clock input/output2 or key scan input5
P44 ($\overline{PWM}$/$\overline{PDO}$/KEY4)			8-bit PWM output or 8-bit programmable divider output or key scan input4
P43 (KEY3) to P40 (KEY0)	I/O (Input)		Key scan inputs 3 to 0
P57 (G8) to P50 (G15)	I/O (Output)	8-bit high breakdown voltage Iinput/output ports with the latch. When used as a VFT driver output, the latch must be cleared to"0".	VFT digit driver outputs
P67 (AIN7) to P60 (AIN0)	I/O (Input)	8-bit programmable input/output port (tri-state).Each bit of the port can be individually configured as an input or an output under software control.	A/D converter analog inputs
P77 (S5/G0) to P72 (S0 / G5)	Output (Output)	Two 8-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	VFT digit/segment driver outputs
P71 (G6) to P70 (G7)			VFT digit driver outputs
P87 (S13) to P80 (S6)	Output (Output)		VFT segment driver outputs
P97 (S21) to P90 (S14)	I/O (Output)	Three 8-bit high breakdown voltage input/output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".	
PD7(S29) to PD0 (S22)			
PE7(S37) to PE0 (S30)			
PF1(S39) to PF0 (S38)		2-bit high breakdown voltage input/output port with latch.When used VFT driver output, the latch most be cleared to "0".	

Pin Name	Input / Output	Function
XIN, XOUT	Input, output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.
$\overline{\text{RESET}}$	I/O	Reset signal input or watchdog timer output / address-trap-reset output / system-clock-reset outputed.
TEST	Input	Test pin for out-going test. Be tied to low.
VDD, VSS (Note)	Power Supply	+ 5 V, 0 V (GND)
VKK		VFT driver power supply
VAREF, VASS		Analog reference voltage inputs (High, Low)

Note: All VDDs should be connected externally for keeping the same voltage level.

OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87CC78/H78/K78/M78. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

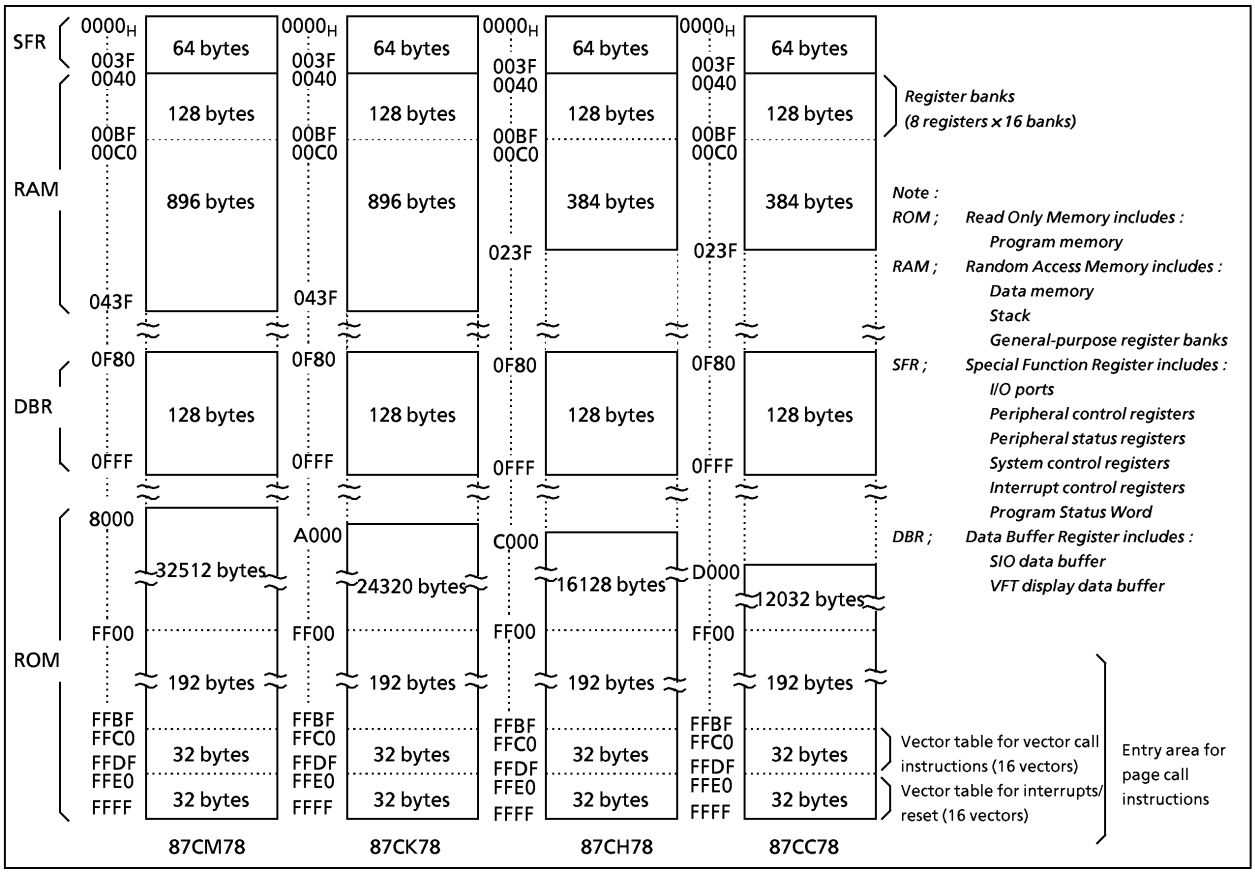


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	P2, P3, P4, P5, P6, XOUT, $\overline{RESET}$	– 0.3 to V_{DD} + 0.3	V
	V_{OUT3}	Source open drain ports	V_{DD} – 40 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	P0, P1, P2, P3, P4, P6	3.2	mA
	I_{OUT3}	P8, P9, PD, PE, PF	– 12	
	I_{OUT4}	P5, P7 (digit outputs)	– 25	
Output Current (Total)	ΣI_{OUT1}	P0, P1, P2, P3, P4, P6	120	mA
	ΣI_{OUT2}	P5, P7, P8, P9, PD, PE, PF	– 240	
Power Dissipation [Topr = 25°C]	PD	Note 2	1200	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: Power Dissipation (PD) ; For PD, it is necessary to decrease 14.3 mw/°C.

Note 3: All VDDs should be connected externally for keeping the same voltage level.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL 1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			fs = 32.768 kHz	SLOW mode	2.7		
				SLEEP mode			
				STOP mode	2.0		
Output Voltage	V_{OUT3}	Source open drain ports			V_{DD} – 38	V_{DD}	V
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 V to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 V to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL 1/2 mode and IDLE 1/2 mode.

How to calculate power consumption.

With the TMP87CC78/CH78/CK78/CM78F, a pull-down resistor (Rk = 80 kΩ typ.) can be built into a VFT driver using mask option (port by port). The share of VFT driver loss (VFT driver output loss + pull-down resistor (Rk) loss) in power consumption Pmax is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption Pd must not be exceeded.

power consumption Pmax = operating power consumption + normal output port loss + VFT driver loss

Where,

operating power consumption	:	VDD x IDD
normal power consumption	:	Σ Iout1 x 0.4
VFT driver loss	:	VFT driver output loss + pull-down resistor (Rk) loss

Example:
When Ta = 10 to 50 °C and a fluorescent display tube with segment output = 3 mA, digit output = 15 mA, Vxx = -25 V is used.
Operating conditions: VDD = 5 V ± 10 %, fc = 8 MHz, VFT dimmer time (DIM) = (14/16) x tseg:

Power consumption Pmax = (1) + (2) + (3)
Where,

(1) Operating power consumption	:	$V_{DD} \times I_{DD}$ = 5.5 V × 16 mA = 88 mW
(2) Normal output port loss	:	Σ Iout1 x 0.4 V = 120 mA × 0.4 V = 48 mW
(3) VFT driver loss	:	segment pin = 3 mA x 2 V x number of segments X = 6 mW x X digit pin = 15 mA x 2 V x 14/16 (DIM) = 26.25 mW Rk loss = $(5.5 + 25\ V)^2$ / 50 kΩ x (number of segments X + 1) = 18.605 mW x (X + 1)

Therefore, Pmax = 88 mW + 48 mW + 6 mW × X + 26.25 mW + 18.605 mWx (X + 1) = 180.855 mW + 24.605X...

Maximum power consumption Pd when Ta = 50 °C is determined by the following equation:
PD = 1200 mW-(14.3 x 25) = 842.5 mW
The number of segments X which can be lit is:
PD > Pmax
842.5 mW > 180.855 + 24.605 X
26 > X

Thus, a fluorescent display tube with less than 26 segments can be used. If a fluorescent display tube with 26 segments or more is used, either a pull-down resistor must be attached externally , or the number of segments to be lit must be kept to less than 26 by software.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain ports, Tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
	I_{IN4}	PD, PE, PF ports (Note3)		–	–	80	
Input Resistance	R_{IN1}	Port P4 with pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Pull-down Resistance	R_K	Source open drain ports	V_{DD} = 5.5V, V_{KK} = – 30 V	50	80	110	
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5 V, V_{OUT} = – 32 V	–	–	– 2	
	I_{LO3}	Tri-state ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V / 0 V	–	–	± 2	
Output High Voltage	V_{OH2}	Tri-state ports	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
	V_{OH3}	P8, P9, PD, PE, PF	V_{DD} = 4.5 V, I_{OH} = – 8 mA	2.4	–	–	
Output Low Voltage	V_{OL}	Except XOUT	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	V
Output High Current	I_{OH}	P5, P7	V_{DD} = 4.5 V, V_{OH} = 2.4 V	–	– 20	–	mA
Supply Current in NORMAL 1, 2 modes	I_{DD}		V_{DD} = 5.5 V fc = 8 MHz fs = 32.768 kHz V_{IN} = 5.3 V / 0.2 V	–	10	16	mA
Supply Current in IDLE 1, 2 modes				–	5	7	
Supply Current in SLOW mode			V_{DD} = 3.0 V fs = 32.768 kHz V_{IN} = 2.8 V / 0.2 V	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V	–	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.
Note 2: Input Current I_{IN1}, I_{IN3}; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.
Note 3: Input Current I_{IN4}; The current when the pull-down register (Rk) is not connected by the mask option.

A/D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	V_{DD} – 1.5	—	V_{DD}	V
	V_{ASS}		V_{SS}	—	1.5	
Analog Input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

Note: Total errors includes all errors, except quantization error.

A.C. Characteristics

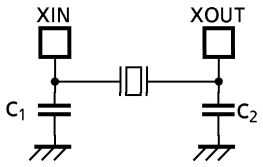
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL1, 2 modes	0.5	–	10	μs
		In IDLE 1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

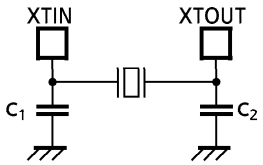
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Oscillator	Oscillation Frequency	Recommended Oscillator		Recommended Constant C_1	Recommended Constant C_2
High-frequency Oscillation	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30pf	30pf
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA 4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20pf	20pf
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency Oscillation	Crystal Oscillator	32.768 KHz	NDK	MX-38T	15pf	15pf



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: An electrical shield by metal shield plate on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.